PL-2501 Hi-Speed USB 2.0 Host-to-Host Bridge/Network Controller

Product Datasheet

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Prolific Technology Inc.

Revision History

Revision	Description	Date
1.1	Modify Table 4-1 (Configurations for Different Operation Modes) to set PL-2501 as default mode.	February 2003
1.0	Add DC Characteristics – Release to Customers	November 2002
0.9	Initial Release – PL2501 Hi-Speed USB 2.0 Host-to-Host Network Bridge Controller	October 2002

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1.0 Introduction

The PL-2501 is a single chip Hi-Speed USB Host-to-Host Bridge Controller. With PL-2501 embedded cable, users can quickly transfer large amount and large size of files directly from one PC to another. Also it's useful for computer data backup/restore, synchronization or file sharing. Additionally, the chip enables two or more Hi-Speed USB or USB1.1 equipped PCs to connect to each other using USB ports as a network. Since Hi-Speed USB extends the speed up to 480 Mbps – 40 times more than previous USB, the network constructed by PL-2501 has data rates almost 5 times faster than a conventional 100BT Ethernet network. Implemented with remote NDIS, users can easily build up this network at a turbo speed without the troubled installation of drivers and add-on network interface cards.

2.0 Features

- Transfer data and share resources between two PCs via USB port
- Full compliance with the Universal Serial Bus Specification Version 1.1 and 2.0
- Supports USB Full/High Speed Control/Interrupt/Bulk Endpoints Transfer
- Supports Suspend, Resume and Remote wake-up power management features
- Embedded Turbo 8032 MCU
- Dual data buffer supporting two-way data transfer
- On-chip USB2.0 UTMI transceiver
- Supports external serial EEPROM to customize vender/product related information
- Supports LED indicator for connection and transfer status
- Bus powered from either USB port
- Suitable for mobile PC environment
- No glue logic needed – can be embedded in small spaces
- 64/100 Pins LQFP packages
- 2.5V operation voltage

3.0 Functional Block

3.1 Block Diagram

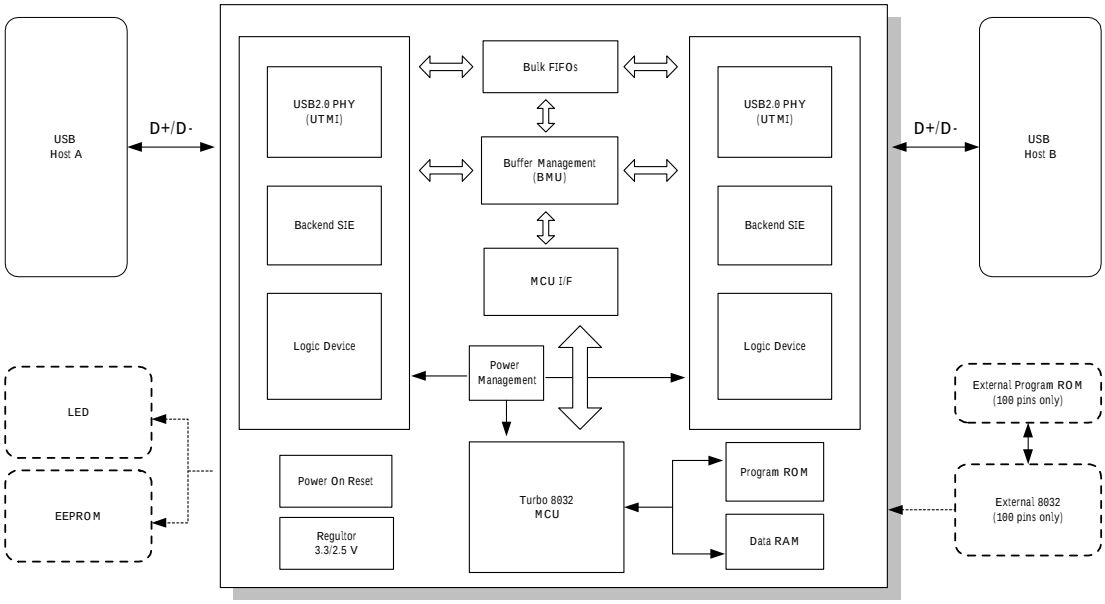

Figure 3-1 Block Diagram

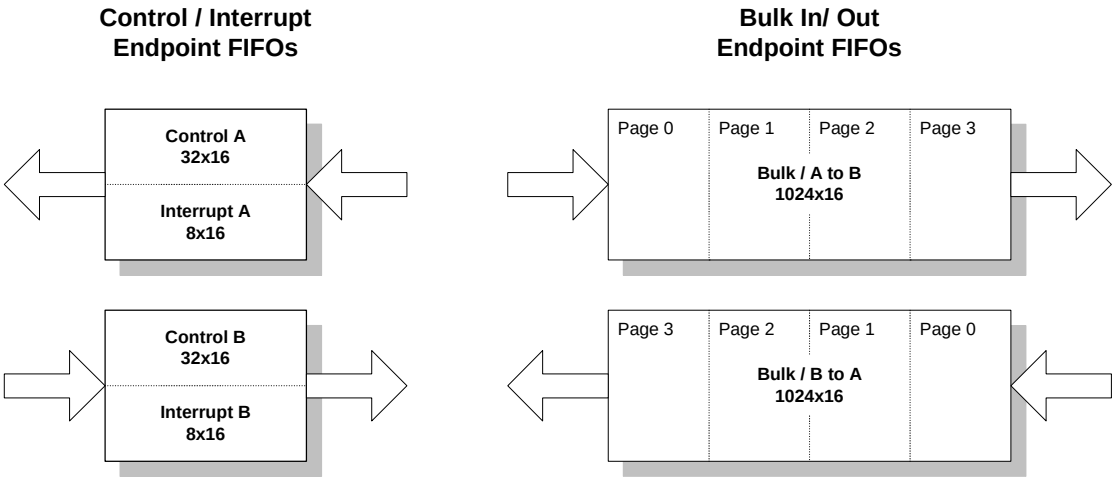

Figure 3-2 FIFO Structure

3.2 Block Description

3.2.1 USB Engine

- USB2.0 PHY. (UTMI)
  Transfer signals between serial D+/D- and parallel 16-bit data.
- Backend SIE
  Handle for CRC and Chirp
- Logic Device
  Decode endpoints and control configuration registers

3.2.2 Core Controller

- Bulk FIFOs
  Provide bi-directional buffers for Bulk Endpoint Transfer
- BMU
  Data flow control for Control/Interrupt/Bulk Transfers, included Control/Interrupt Endpoints FIFOs.
- MCU I/F
  This is responsible for accessing internal Data RAM and communicating between Core Controller and Turbo 8032 MCU.
- Power Management
  Service for Suspend / Wakeup / RemoteWakeup and Turbo 8032 MCU clock switch.

3.2.3 Embedded CPU

- MCU Turbo 8032
- Program ROM Size is 12Kx8 for default Program
- Data RAM Size is 64-Byte for extra usage

3.2.4 Miscellaneous

- POR Power On Reset module
- REG Regulator 3.3/2.5 V

4.0 System Description

With a link cable embedded with the PL-2501 circuit board, users can easily transfer large amount and size of files directly from one PC to another without having to transfer the files to an intermediary data storage. The PL-2501 is also useful for computer data backup/restore, synchronization or file sharing. This chip solution is especially suitable for those who need bulk data transfer between one notebook PC and desktop PC. The PL-2501 also includes two 2K-byte FIFO (4 pages of USB 2.0 Bulk Endpoint max. package size - 512 bytes) for bi-directional Bulk transfer to achieve the highest throughput of USB 2.0 Hi-Speed bandwidth.

4.1 Operation Modes

There are 4 different operation modes for the PL-2501:

- **2301 mode (PL-2301 compatible mode):**
  This is suitable for customers who still want to use the PL-2301 driver and PClinq USB-to-USB data transfer AP while running at a higher data transfer rate (12Mb/s to 480Mb/s).

- **2302 mode for NDIS networking:**
  This is suitable for customers who still want to use the PL-2302 network (NDIS) driver and AP while running at a higher data transfer rate (12Mb/s to 480Mb/s).

- **2501 mode (not compatible with PL-2301):**
  This mode uses the new PL-2501 user-friendly AP (Pclinq2) interface and advanced protocol. Users can gain the benefits of higher bandwidth and data transfer rate than PL-2301.

- **2502 mode for Remote NDIS networking:**
  Fully compliant to Remote NDIS Specification, users can communicate two PCs just by plug & play two USB ports. There is no need to install drivers, add-in network card and setup tedious network environment. Users can share programs, files, and peripheral equipment easily.

The operation modes are dependent on the configuration of pin P1[0] and P1[1] as follows:

Table 4-1 Configurations for Different Operation Modes

Mode	P1[1]	P1[0]	Description
2301	0	1	Support PL2301 AP & Driver
2302	1	0	Support PL2302 NDIS
2501	1	1	Support PL2501 AP & Driver
2502	0	0	Support PL2502 Remote NDIS

5.0 Pin Assignment and Description

5.1 Pin Assignment and Description of PL-2501 LQFP100

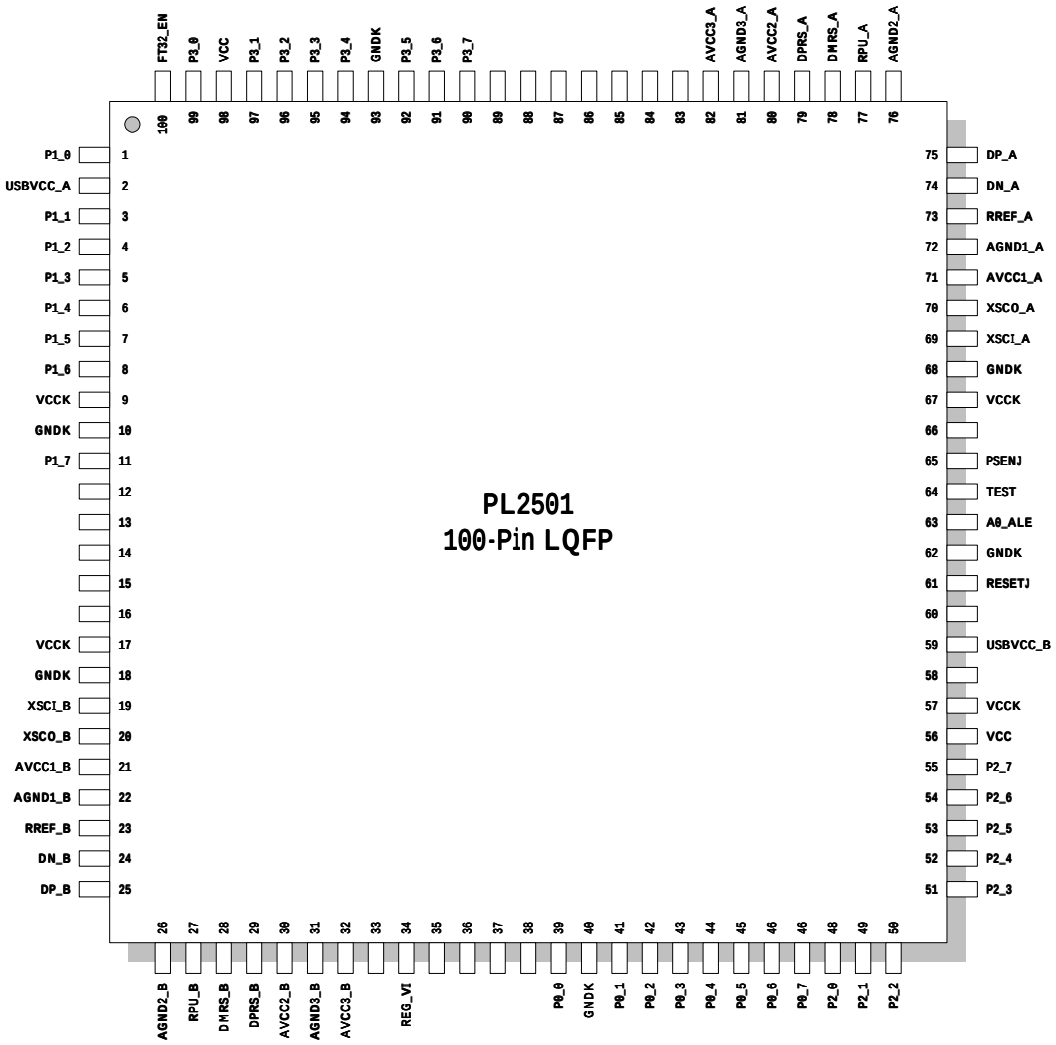

Figure 5-1 Pin Assignment of PL-2501 LQFP100

5.2 Pin Assignment and Description of PL-2501 LQFP64

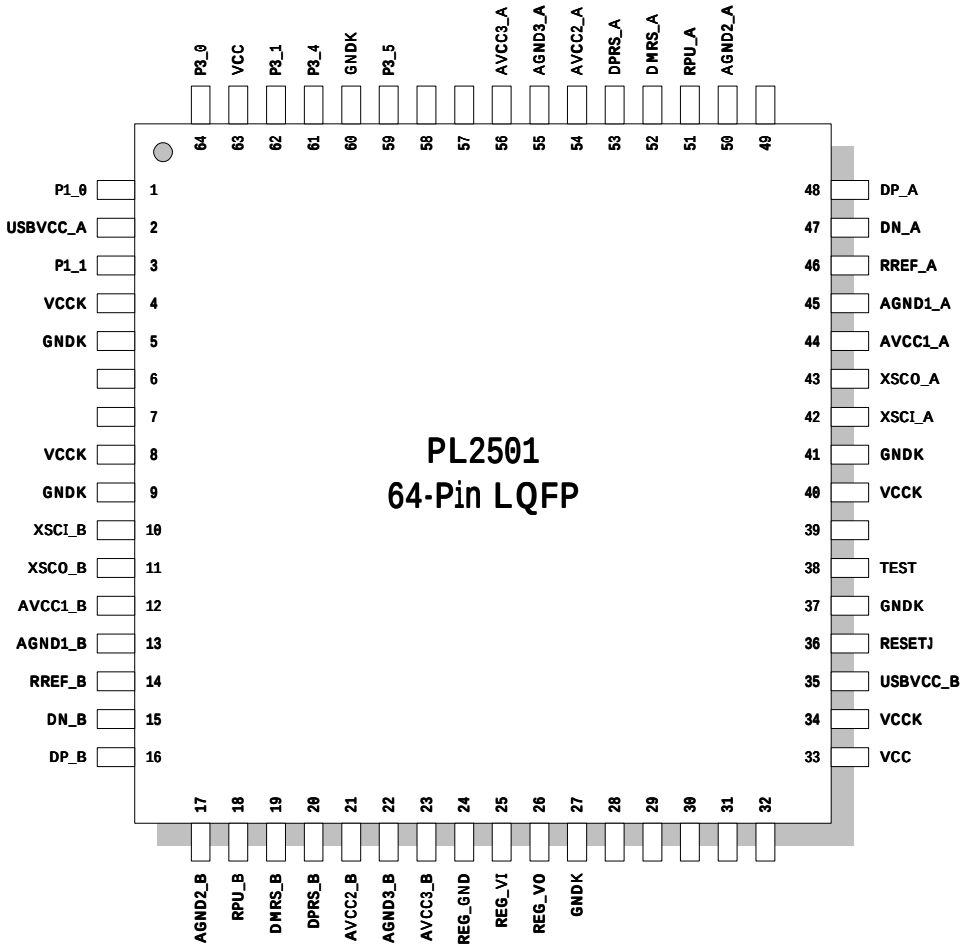

Figure 5-2 Pin Assignment of PL-2501 LQFP64

The following table describes each pin:

I – Input signal O – Output signal I/O – Bi-directional signal

P – Power/Ground N – No connect

Table 5-1 USB2.0 Phy_A related pins

Name	Pin No (100)	Pin No (64)	Type	Description
XSCI_A	69	42	I	Clock in or CMOS oscillator input.
XSCO_A	70	43	O	CMOS oscillator output.
RREF_A	73	46	A	PLL Reference level
DP_A	75	48	I/O	High speed DPLUS signal
DN_A	74	47	I/O	High speed DMINUS signal
RPU_A	77	51	A	1.5 K ohm Pull-up resistor
DPRS_A	79	53	I/O	Full speed DPLUS signal
DMRS_A	78	52	I/O	Full speed DMINUS signal
VCCK	67	40	P	Digital Power 2.5v
GNDK	68	41	P	Digital Ground
AVCC1_A, AVCC2_A, AVCC3_A	71, 80, 82	44, 54, 56	P	Analog Power 3.3v for on-chip PHY
AGND1_A, AGND2_A, AGND3_A	72, 76, 81	45, 40, 55	P	Analog Ground for on-chip USB PHY.

Table 5-2 USB2.0 Phy_B related pins

Name	Pin No (100)	Pin No (64)	Type	Description
XSCI_B	19	10	I	Clock in or CMOS oscillator input.
XSCO_B	20	11	O	CMOS oscillator output.
RREF_B	23	14	A	PLL Reference level
DP_B	25	16	I/O	High speed DPLUS signal
DN_B	24	15	I/O	High speed DMINUS signal
RPU_B	27	18	A	1.5 K ohm Pull-up resistor
DPRS_B	29	20	I/O	Full speed DPLUS signal
DMRS_B	28	19	I/O	Full speed DMINUS signal
VCCK	17	8	P	Digital Power 2.5v
GNDK	18	9	P	Digital Ground

Table 5-2 USB2.0 Phy_B related pins (cont…)

Name	Pin No (100)	Pin No (64)	Type	Description
AVCC1_B, AVCC2_B, AVCC3_B	21, 30, 32	12, 21, 23	P	Analog Power 3.3v for on-chip PHY
AGND1_B, AGND2_B, AGND3_B	22, 26, 31	13, 17, 22	P	Analog Ground for on-chip USB PHY.

Table 5-3 Internal 8032 MCU related pins

Name	Pin No (100)	Pin No (64)	Type	Description
P0[7:0]	47~41, 39	N/A	I/O	Reserved for external 8032
P1[7:2]	11,8~4	N/A	1/O	Reserved for GPIO
P1[1:0]	3,1	3,1	I/O	00: 2301 mode 01: 2302 mode 10: 2501 mode 11: 2502 mode
P2[7:0]	55~48	N/A	I/O	Reserved for external 8032
P3[7:6]	90~91	N/A	I/O	Reserved for external 8032
P3[5:4]	92,94	59,61	I/O	EE_CLK: P3[5] EE_DATA: P3[4]
P3[3:2]	95,96	N/A	I/O	Reserved for external 8032
P3[1:0]	97,99	62,64	I/O	LED_TRAN: P3[1] LED_CNNT: P3[0]
PSENJ	65	N/A	I/O	Reserved for external 8032
A0_ALE	63	N/A	I/O	Reserved for external 8032

Table 5-4 System Pins

Name	Pin No (100)	Pin No (64)	Type	Description
REG_VI	34	25	P	REG Power In: 3.3v Power pin for on-chip 3.3v/2.5v regulator
REG_GND	33	24	P	REG Ground: pin for on-chip 3.3v/2.5v regulator
REG_VO	35	26	P	REG Power Out2.5v power output of 3.3v/2.5v regulator
RESETJ	61	36	I	External reset pin. Low active.

Table 5-4 System Pins (cont…)

Name	Pin No (100)	Pin No (64)	Type	Description
TEST	64	38	I	Chip Test mode enable. Internal PAD pull down.
USBVCC_A	2	2	I	USBVCC_A,
USBVCC_B	59	35	I	USBVCC_B,
FT32_EN	100	N/A	I	FT32_EN, internal 8032 MCU enable Internal PAD pull up.
VCC	56, 98	33, 63	P	3.3v Power pins
VCCK	9, 57	4, 34	P	2.5v Power pins
GNDK	10,40, 62,93	5,27, 37,60	P	Digital ground pins
NC	12~16, 36~38, 58, 60, 66, 83~89	6~7, 28~32, 39, 57~58	N	No connection.

6.0 DC Characteristics

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	2.5V Power Supply	-0.3 to 3.0	V
	3.3V Power Supply	-0.3 to 3.9	
V_{IN2}	Input Voltage of 2.5V I/O	-0.3 to V_{CC2I} +0.3	V
	Input Voltage of 2.5V I/O with 3.3V Tolerance	-0.3 to 3.9	
V_{IN3}	Input Voltage of 3.3V I/O	-0.3 to V_{CC3I} +0.3	V
	Input Voltage of 3.3V I/O with 5V Tolerance	-0.3 to 5.5	
T_{STG}	Storage Temperature	-40 to 150 (TBD)	^{o}C

6.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC21}	Power Supply of 2.5V I/O	2.25	2.5	2.75	V
V_{CC3I}	Power Supply of 3.3V I/O	3.0	3.3	3.6	V
T_J	Commercial Junction Operating Temperature	0	25	115	^{o}C
	Industrial Junction Operating Temperature	-40	25	125	

6.3 Leakage Current and Capacitance(3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Leakage Current$_{(2)}$	no pull-up or pull-down	-10		10	uA
C_{IN2}	Input Capacitance			3.1		pF
C_{OUT2}	Output Capacitance			3.1		pF

(1) Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

(2) The pull up/pull down input leakage current can be derived from the pull up/pull down resistance (Rpu/Rpd) in the DC characteristics table for each type I/O buffer.

(3) The capacitances listed above do not include PAD capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance's that is about 0.1pF and the package capacitance.

6.4 DC Characteristics of 2.5V Programmable I/O Cells

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC21}	Power Supply	2.5V I/O	2.25	2.5	2.75	V
V_{IL}	Input Low Voltage	CMOS			0.3*VCC	V
V_{IH}	Input High Voltage	CMOS	0.7*VCC			V
I_{IN}	Input Leakage Current	Vin=0 or VCC21	-10		10	uA

6.5 DC Characteristics of 3.3V Programmable I/O Cells

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC31}	Power Supply	3.3V I/O	3.0	3.3	3.6	V
V_{IL}	Input Low Voltage*	CMOS/LVTTL			0.8	V
V_{IH}	Input High Voltage*	CMOS/LVTTL	2.0			V
I_{IN}	Input Leakage Current	Vin=0 or VCC31	-10		10	uA

7.0 Outline Diagram

7.1 LQ100 Package

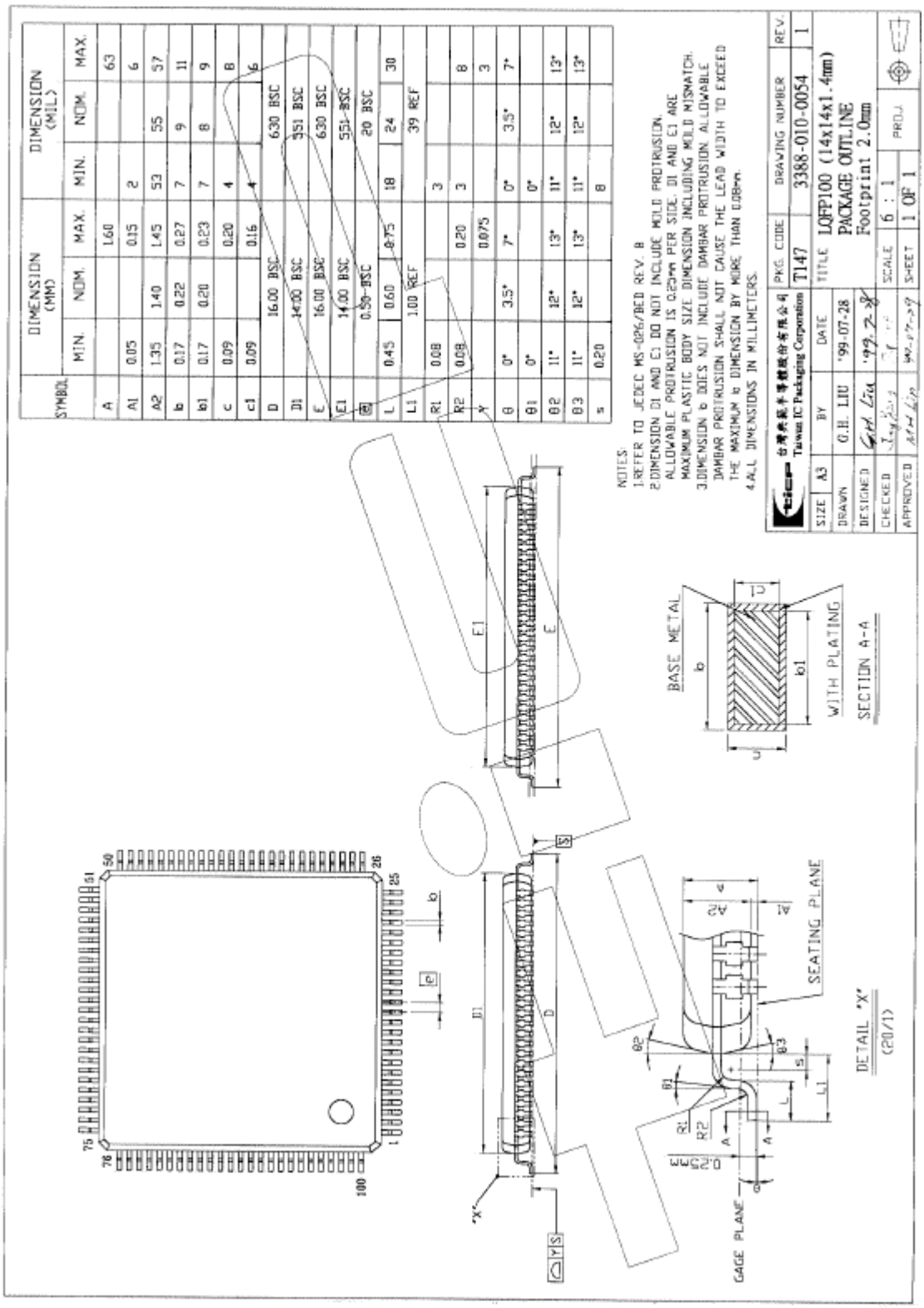

Figure 7-1 Outline Diagram of PL-2501 LQFP100

7.2 LQ64 Package

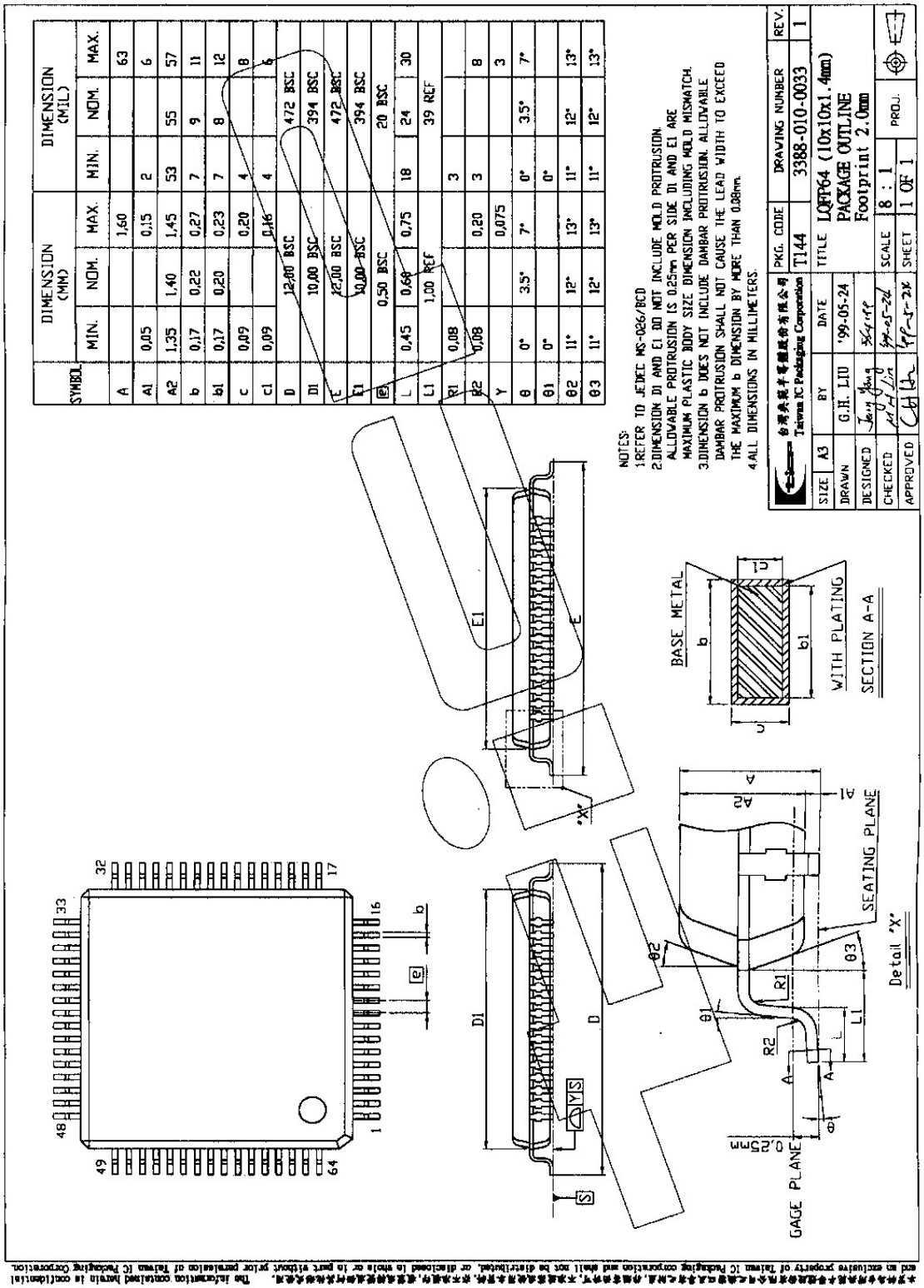

Figure 7-2 Outline Diagram of PL-2501 LQFP64