XFBL-XXYY96-40D
10Gb/s BIDI XFP 40km Transceiver

PRODUCT FEATURES

- Hot-pluggable XFP footprint
- Supports 9.95Gb/s to 11.3Gb/s bit rates
- XFI Loopback Mode
- RoHS-6 Compliant (lead-free)
- 1270nm DFB laser and PIN receiver for XFBL-273396-40D

  1330nm DFB laser and PIN receiver for XFBL-332796-40D
- Power dissipation<2W
- Case operating temperature 0 ºC~70ºC
- Up to 40km transmission on SMF
- 2-wire interface with integrated Digital Diagnostic monitoring
- EEPROM with Serial ID Functionality
- Compliant with XFP MSA with LC connector

APPLICATIONS

- 10GBASE-BX 10.3125Gb/s Ethernet
- 10GBASE-BX 9.953Gb/s Ethernet
- SONET OC-192 &SDH STM I-64.1

PRODUCT DESCRIPTION

XFBL-XXYY96-40D is hot pluggable 3.3V Small-Form-Factor transceiver module. It designed expressly for high-speed communication applications that require rates up to 11.3Gb/s, it designed to be compliant with XFP MSA. The module data link up to 40km in 9/125um single mode fiber.

Ⅰ. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	Ts	-40	-	85	℃	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.3	-	4	V	
Signal Input Voltage	VCC	Vcc-0.3	-	Vcc+0.3	V	

Ⅱ. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	Tcase	0	-	70	℃	Without air flow
Power Supply Voltage	VCC	3.14	3.3	3.47	V	
Power Supply Current	ICC	-	-	600	mA	
Data Rate	BR	9.95	10.3125	11.3	Gbps	
Transmission Distance	TD	2	-	40	km	
Coupled fiber	Single mode fiber					

Ⅲ. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Average Launched Power	Pout	0	-	5	dBm	
Average Launch power of OFF transmitter	P_{OFF}	-	-	-30	dBm	Note (1)
Centre Wavelength Range	λC	1260	1270	1280	nm	XFBL-273396-40D
		1320	1330	1340	nm	XFBL-332796-40D
Side mode suppression ratio	SMSR	30	-	-	dB	
Spectrum Bandwidth(-20dB)	σ	-	-	1	nm	
Extinction Ratio	ER	3.5		-	dB	Note (2)
Output Eye Mask	Compliant with IEEE 802.3ae requirements					Note (2)
Receiver						
Input Optical Wavelength	λIN	1320	1330	1340	nm	XFBL-273396-40D
		1260	1270	1280	nm	XFBL-332796-40D
Receiver Sensitivity in average	Psen	-	-	-15	dBm	Note (3)
Input Saturation Power (Overload)	PSAT	0.5	-	-	dBm	Note (3)
LOS -Assert Power	PA	-32	-	-	dBm	
LOS -Deassert Power	PD	-	-	-18	dBm	

LOS -Hysteresis	PHys	0.5	-	4	dB	

Note:
1. The optical power is launched into SMF
2. Measured with RPBS 2^31-1 test pattern @10.3125Gbs
3. Measured with RPBS 2^31-1 test pattern @10.3125Gbs BER=<10^-12

IV. Electrical Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Total power supply current	Icc	-	-	600	mA	
Transmitter						
Differential Data Input Voltage	VDT	120	-	820	mVp-p	
Differential line input Impedance	RIN	85	100	115	Ohm	
Transmitter Fault Output-High	VFaultH	2.4	-	Vcc	V	
Transmitter Fault Output-Low	VFaultL	-0.3	-	0.8	V	
Transmitter Disable Voltage- High	VDisH	2	-	Vcc+0.3	V	
Transmitter Disable Voltage- low	VDisL	-0.3	-	0.8	V	
Receiver						
Differential Data Output Voltage	VDR	300	-	850	mVp-p	
Differential line Output Impedance	ROUT	80	100	120	Ohm	
Receiver LOS Pull up Resistor	RLOS	4.7	-	10	KOhm	
Data Output Rise/Fall time	tr/tf	20	-	-	ps	
LOS Output Voltage-High	VLOSH	2	-	Vcc	V	
LOS Output Voltage-Low	VLOSL	-0.3	-	0.4	V	

V. Pin Assignment

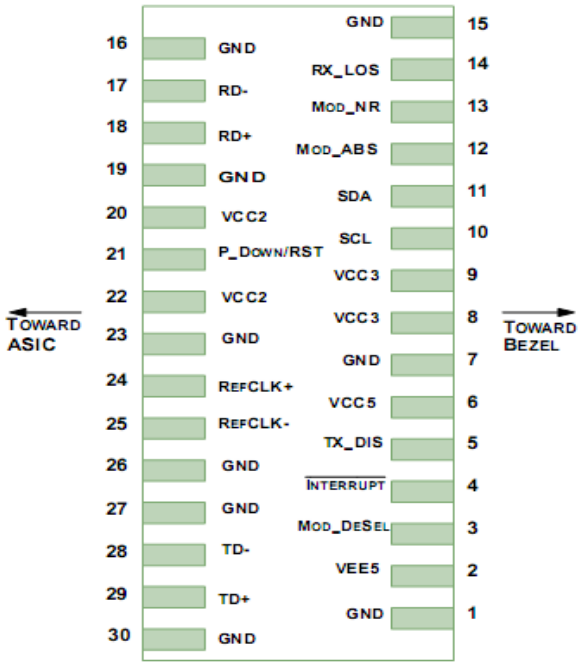


Diagram of Host Board Connector Block Pin Numbers and Name

Pin	Logic	Symbol	Name/Description	Note
1		GND	Module Ground	1
2		VEE5	Optional –5.2 Power Supply – **Not required**	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	
4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTLI/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready; XGIGA defines it as a logical OR between RX_LOS and Loss of Lock in TX/RX.	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply – **Not required**	

21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply – **Not required**	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – **Not required**	3
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – **Not required**	3
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10kohms on host board to a voltage between 3.15V and 3.6V.
3. A Reference Clock input is not required by the XFBL-XXYY96-40D. If present, it will be ignored.

VI. Digital Diagnostic Functions

As defined by the XFP MSA, XGIGA XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

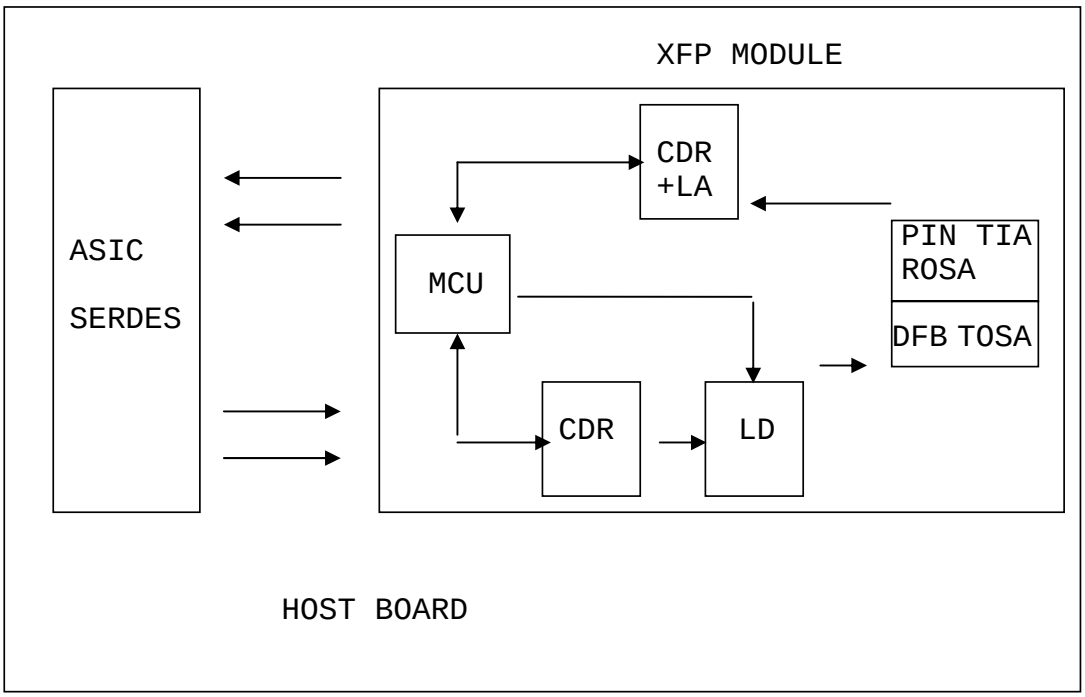
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit

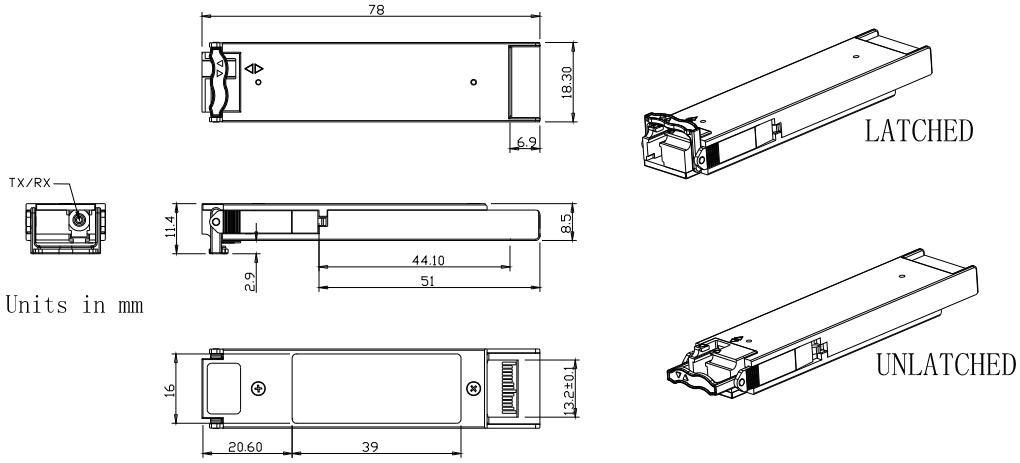
parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the XFP MSA Specification.

VII. Recommended Block Circuit



VIII. Outline Dimensions



IX. Regulatory Compliance

Feature	Reference	Performance
Electrostatic discharge（ESD）	IEC/EN 61000-4-2	Compatible with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN 55022 Class B (CISPR 22A)	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10, 1040.11 IEC/EN 60825-1，2	Class 1 laser product
Component Recognition	IEC/EN 60950 ，UL	Compatible with standards
ROHS	2002/95/EC	Compatible with standards
EMC	EN61000-3	Compatible with standards

Appendix A. Document Revision

Version No.	Date	Description
1.0	2010-09-01	Preliminary datasheet
2.0	2011-09-10	Update format and company’s logo